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(71) Applicant: LSI LOGIC CORPORATION
1551 McCarthy Boulevard
Milpitas, CA 95035 (US)

(72) Inventor: Boruta, Mirek
2529 Nordell Avenue,
Castro Valley California 94546 (US)

(74) Representative: Barnard, Eric Edward
BROOKES & MARTIN
High Holborn House
52/54 High Holborn
London WC1V 6SE (GB)

(54) **Multicut wafer saw process.**

(57) A method of cutting a plate-like wafer (30), particularly a semiconductor wafer, while removing a deposited material (32) from along a scribe line. The deposited material having a width generally greater than the width of the saw blade (33). The method includes making one scribing cut (36) to one side of the scribe line, making a second scribing cut (38) to the other side of the scribe line, and making a severing cut (39) along the scribe line to dice the wafer.

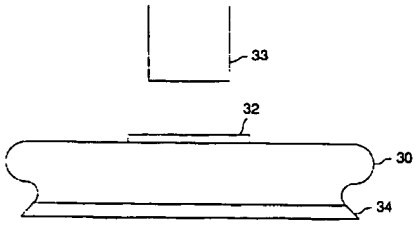


FIG. 2A

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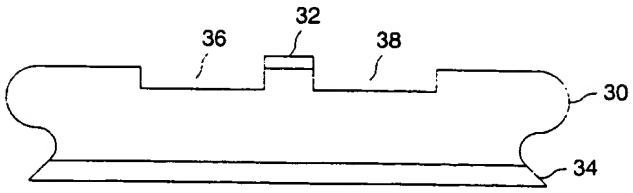


FIG. 2C


FIG. 2D

## BACKGROUND OF THE INVENTION

The present invention relates generally to a method for cutting a plate-like material and, more specifically, to a method of cutting a semiconductor wafer that contains metal deposits along a scribe line.

In the manufacture of semiconductor devices, multiple semiconductor devices are typically arranged on one surface of a round silicon wafer. It is known to separate or dice the multiple semiconductor devices with a diamond coated saw blade along the scribe line.

However, semiconductor wafers may have test patterns deposited along the scribe line on the surface of the wafer. These test patterns may be composed of metal and have a width wider than the width of the standard diamond saw blade. After the wafer is cut, metal may remain on the edge of the cut and metal slivers may subsequently become dislodged. The slivers can interfere with the operation of the semiconductor device and thus affect the reliability of the device.

## SUMMARY OF THE INVENTION

The present invention provides a method for cutting semiconductor wafers that contain test patterns on the scribe lines without producing slivers. The present invention uses multiple scribing cuts to remove the excess test pattern material, followed by a severing cut to dice the semiconductor wafer along the scribe line and remove any test pattern material that may remain.

In an embodiment of the present invention, the test patterns are removed by scribing cuts made with a beveled or V-shaped blade. The semiconductor wafer is then severed along the scribe line with a standard flat surface saw blade.

A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B show a method of cutting a semiconductor wafer according to the prior art;

Fig. 1A is a cross sectional view of a semiconductor wafer cut before being cut;

Fig. 1B is a cross sectional view of a semiconductor wafer after being cut;

Figs. 2A through 2D show a method of cutting a semiconductor wafer according to an embodiment of the present invention;

Fig. 2A is a cross sectional view of a semiconductor wafer before being cut;

Fig. 2B is a cross sectional view of a semiconductor wafer after a first scribing cut;

Fig. 2C is a cross sectional view of a semiconductor wafer after a second scribing cut;

Fig. 2D is a cross sectional view of a semiconductor wafer after a third severing cut;

Figs. 3A though 3D show a method of cutting a semiconductor wafer according to an embodiment of the present invention;

Fig. 3A is a cross sectional view of a semiconductor wafer before being cut;

Fig. 3B is a cross sectional view of a semiconductor wafer after a first scribing cut;

Fig. 3C is a cross sectional view of a semiconductor wafer after a second scribing cut;

Fig. 3D is a cross sectional view of a semiconductor wafer after a third severing cut;

Figs. 4A through 4D show a method of cutting a semiconductor wafer according to an embodiment of the present invention;

Fig. 4A is a cross sectional view of a semiconductor wafer before being cut;

Fig. 4B is a cross sectional view of a semiconductor wafer after a first scribing cut;

Fig. 4C is a cross sectional view of a semiconductor wafer before a second severing cut;

Fig. 4D is a cross sectional view of a semiconductor wafer after a second severing cut;

Figs. 5A and 5B show a method of cutting a semiconductor wafer according to an embodiment of the present invention;

Fig. 5A is a cross sectional view of a semiconductor wafer cut before being cut;

Fig. 5B is a cross sectional view of a semiconductor wafer cut after being cut.

## DESCRIPTION OF SPECIFIC EMBODIMENTS

The examples of specific embodiments of the present invention describe making first, second, and third cuts in the semiconductor wafer. It should be understood, however, that these designations are for convenience, and should not be taken to mean that the cuts must be performed in any defined order. Similarly, the number of cuts can be more or less than shown in the specific embodiments described herein.

### Dicing Method According to the Prior Art

Figs. 1A and 1B show a prior art method of cutting a semiconductor wafer. In Fig. 1A, a semiconductor wafer 10 has a metal test pattern 12 deposited on the surface of the wafer. The test pattern may be deposited along an area known as a scribe line. A scribe line or street is the area between semiconductor devices where a diamond saw blade 13 will sever or dice the semiconductor wafer. The saw blade will generally have a width less than the width of the scribe line. Typically the saw blade has a blade thickness of 1.2 to 1.6 mil.

The semiconductor wafer is shown having a layer of mounting tape 14 taped to the underside of the wafer. The mounting tape is attached to a frame (not shown) and secures the wafer die both during and after the cutting process. The saw blade does not sever the mounting tape.

Fig. 1B shows the semiconductor wafer after it has been cut according to the prior art. The cut severs the semiconductor wafer in the middle of the scribe line creating a groove 16. As the width of the test patterns may be wider than the saw blade, two portions of test pattern 12 remain on the top surface of the wafer near groove 16. These portions of the test pattern may become dislodged as slivers and affect the reliability of the packaged semiconductor device. This is especially true when the test pattern is composed of a conducting material because the slivers may short out the semiconductor device.

Multi Cut Dicing Method According to the Present Invention

In an embodiment of the present invention shown in Figs. 2A through 2D, two scribing cuts are used to eliminate portions of the test pattern and a third severing cut dices the wafer, removing whatever portion, if any, of the test pattern that remains.

In Fig. 2A, a semiconductor wafer 30 has a metal test pattern 32 deposited along the scribe line on the surface of the wafer. A standard flat surface saw blade 33 is used to cut the wafer. A mounting tape 34 is taped to the underside of the semiconductor wafer and attached to a frame (not shown).

A first scribing cut is made in the semiconductor wafer on one side of the scribe line to remove a first portion of test pattern 32. Fig. 2B shows the wafer after the first scribing cut which leaves a groove 36. Then a second scribing cut is made in the semiconductor wafer on the other side of the scribe line to remove a second portion of test pattern 32. The second cut leaves a groove 38 and is shown in Fig. 2C. Neither the first or second scribing cuts sever the wafer and are only intended to remove portions of the test pattern outside the width of the saw blade. Thus, the first and second cuts may be superficial.

A third severing cut is then made along the center of the scribe line to sever the wafer. Fig. 2D shows the wafer after the third cut which leaves a groove 39. The cut severs the wafer but does not sever mounting tape 34. Although the description and figures show the third severing cut passing through the wafer, the present invention may also be practiced where the third cut does not sever the wafer. The wafer may then be broken along the scribe line in any number of ways known to those skilled in the art.

The following are an example of machine settings for practicing the above-described multi cut dicing method:

| | cut depth | max. feed speed |
|---|---|---|
| first cut | 3 mils | 0.5 in./second |
| second cut | 3 mils | 0.5 in./second |
| third cut | 18.5 mils | 2.5 in./second |

These settings are for a standard semiconductor wafer and may be modified for other uses.

In another embodiment of the present invention shown in Figs. 3A through 3D, two scribing cuts are made with a beveled or V-shaped saw blade to remove the test pattern. A third severing cut is made with a standard flat surface blade to sever the wafer.

In Fig. 3A, a semiconductor wafer 60 has a metal test pattern 62 deposited along the scribe line on the surface of the wafer. A V-shaped saw blade 63 is used to scribe the wafer along the scribe line. A mounting tape 64 is taped to the underside of the semiconductor wafer.

A first scribing cut is made in the semiconductor wafer along one half of the scribe line to remove a first portion of test pattern 62. Fig. 3B shows the wafer after the first scribing cut which leaves a groove 68. Then a second scribing cut is made in the semiconductor wafer along the other half of the scribe line to remove a second portion of test pattern 62. The second scribing cut leaves a groove 70 and is shown in Fig. 3C. Neither the first or second scribing cuts sever the wafer and are only intended to remove the test pattern.

A third severing cut is then made along the scribe line to sever the wafer. Fig. 3D shows the wafer after the third severing cut. The third cut may be made with a standard flat surface saw blade 72 leaving a groove 74. The third cut severs the wafer but does not sever mounting tape 64. This embodiment has the advantage of producing beveled top edges along the scribe line. Beveled edges help reduce semiconductor wafer chipping.

In another embodiment of the present invention shown in Figs. 4A through 4D, one scribing cut is made with a V-shaped saw blade to remove the test pattern. The saw blade has a thickness greater than the width of the test pattern. A second severing cut is made with a flat surface saw blade to sever the wafer.

In Fig. 4A, a semiconductor wafer 80 has a metal test pattern 82 deposited along the scribe line on the surface of the wafer. A V-shaped saw blade 83 is used to scribe the wafer along the scribe line. The saw blade has a thickness greater than the width of the test pattern so only one cut is needed to scribe the test pattern. A mounting tape 84 is taped to the underside of the semiconductor wafer.

A first scribing cut is made in the semiconductor wafer to remove test pattern 82. Fig. 4B shows the wafer after the first scribing cut which leaves a groove

86. Then a second severing cut is made along the scribe line to dice the wafer. Fig. 4C shows a flat surface saw blade 88 may be used to make the second severing cut. Fig. 4D shows the wafer after the second severing cut which leaves a groove 90. The second severing cut severs the wafer but does not sever mounting tape 84. This embodiment also has the advantage of producing beveled top edges along the scribe line which may help reduce semiconductor wafer chipping.

Single Cut Dicing Method According to the Present Invention

The present invention may also be practiced where a single scribing/severing cut is made with a V-shaped saw blade which has a thickness greater than the width of the test pattern. This method is shown in Figs. 5A and 5B.

In Fig. 5A, a semiconductor wafer 100 has a metal test pattern 102 deposited along the scribe line on the surface of the wafer. A V-shaped saw blade 103 is used to scribe and sever the wafer along the scribe line. As the saw blade has a thickness greater than the width of the test pattern, the severing cut can also scribe the test pattern. A mounting tape 104 is taped to the underside of the semiconductor wafer.

A first scribing/severing cut is made in the semiconductor wafer to remove test pattern 102 and sever the wafer. Fig. 4B shows the wafer after the first scribing/severing cut which leaves a groove 106. The scribing/severing cut severs the wafer but does not sever mounting tape 104. This embodiment also has the advantage of producing beveled top edges along the scribe line which may help reduce semiconductor wafer chipping.

Conclusion

The above description of the embodiments of the invention is intended as illustrative rather than inclusive. Modification of the invention as to number of cuts, surface of the saw blade, depth of the cuts, and cutting speed is likely and such modifications are still within the intended scope of protection of the invention which is defined by the following appended claims.

**Claims**

1. A method of cutting a semiconductor wafer (30,60,80) along a scribe line with a saw blade (33,63,83), said scribe line being located on a top surface of said wafer which has a test pattern (32,62,82) deposited above said scribe line; said method comprising the steps of:

   making at least one scribing cut (36,38,68,70,86) into the top surface of said wafer containing said test pattern and

   making a severing cut (39,74,90) along the scribe line to remove the remaining test pattern and to sever said wafer.

2. A method of cutting a semiconductor wafer (100) along a scribe line with a V-shaped blade (103), said scribe line being located on a top surface of said wafer which has a test pattern (102) deposited above said scribe line; said method comprising the step of making a cut (106) into the top surface of said wafer to both scribe said test pattern and sever said wafer; said saw blade (103) having a thickness greater than the width of said test pattern (102).

3. A method according to claim 1, wherein said severing cut (39,74,90) only partially servers said semiconductor wafer.

4. A method according to claim 3, and further comprising the step of breaking said semiconductor wafer along said severing cut (39,74,90).

5. A method according to any one of claims 1,3 or 4 wherein the at least one scribing cut (36,38) is made with a saw blade (33), and the width of the test pattern remaining after said at least one scribing cut (36,38) is not greater than the thickness of the saw blade (33).

6. A method according to any one of claims 1,3 or 4 wherein said at least one scribing cut (68,70,86) removes said test pattern.

7. A method according to any one of claims 1,3 or 4 wherein said at least one scribing cut comprises the steps of: making a first scribing cut (36,68) along one side of said scribe line and

   making a second scribing cut (38,70) along the other side of said scribe line.

8. A method according to claim 7, wherein the first and second scribing cuts (36,68,38,70) remove the test pattern (32,62).

9. A method according to any of one claims 1 to 8, further comprising the steps of applying mounting tape (34,64,84,104) to the underside of said semiconductor wafer (30,60,80,100) prior to the cutting thereof.

10. A method according to claim 9 wherein the severing cut (39,74,90,106) severs said semiconductor wafer (30,60,80,100) without severing said mounting tape (34,64,84,104).

11. A method according to any one of claims 1,3,4,5,6,7 or 8 wherein said at least one severing cut (39, 74) is made with a flat surface saw blade (33,72,88).

12. A method according to any one of claims 1,3,4,5,6,7 or 8 wherein the scribing and severing cuts (68,70,74,86,90) are made with separate saw blades (63,72,83,88).

13. A method according to any one of claims 1,3,4,5,6,7,8 or 12 wherein the at least one scribing cut (68,70,86) is made with a V-shaped blade (63,83) and the severing cut (74,90) is made with a flat blade (72,88).

14. A method according to any one of claims 1 to 13, wherein the scribing and severing cuts (36,38,68,70,86,39,74,90,106) are made at substantially perpendicular angles to the top surface of said semiconductor wafer (30,60,80,100).

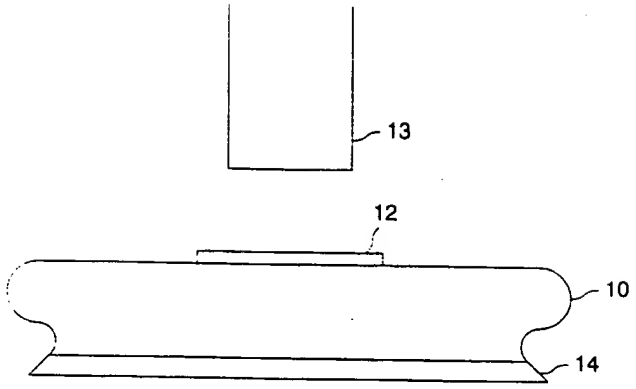


*FIG. 1A*
PRIOR ART

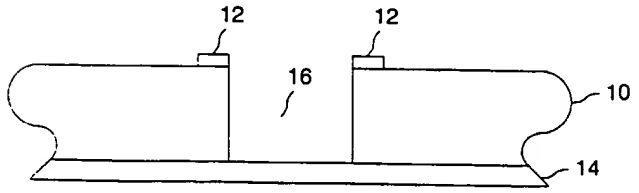


*FIG. 1B*
PRIOR ART

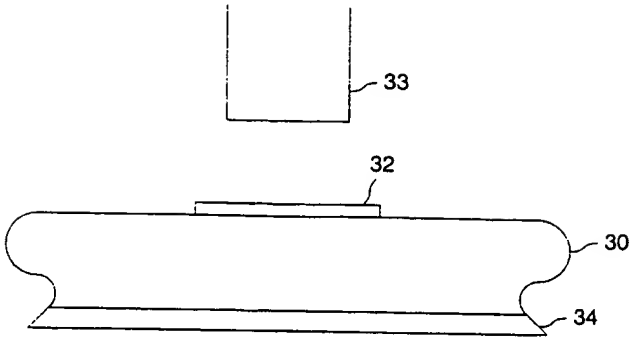


FIG. 2A

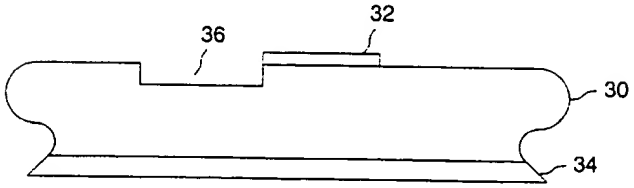


FIG. 2B

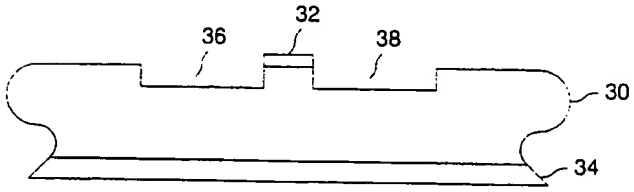


FIG. 2C

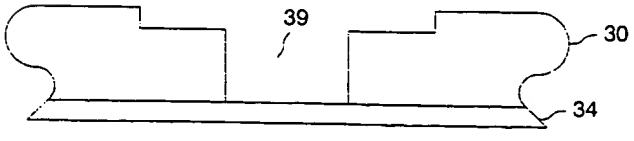


FIG. 2D

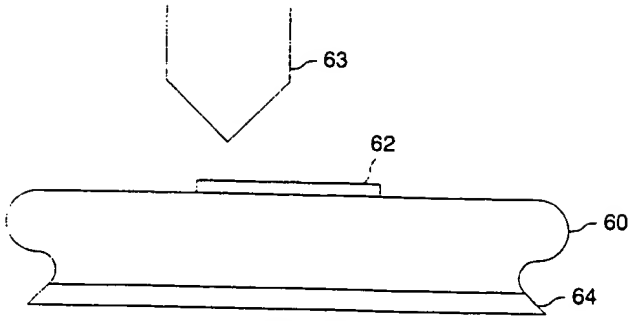


FIG. 3A

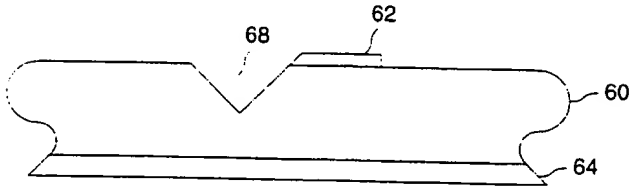


FIG. 3B

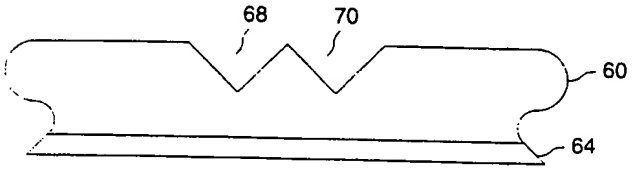


FIG. 3C

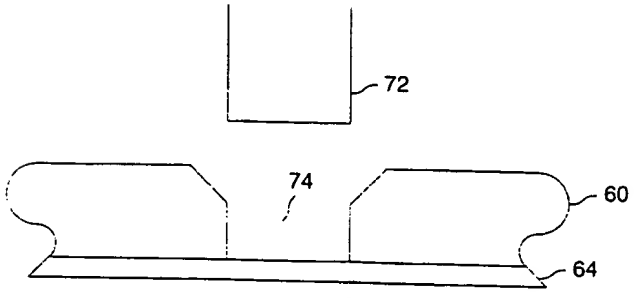


FIG. 3D

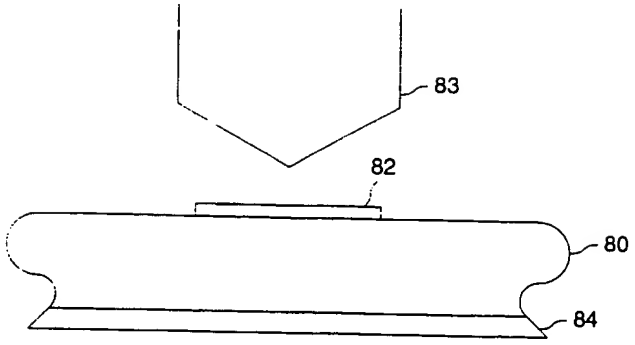


FIG. 4A

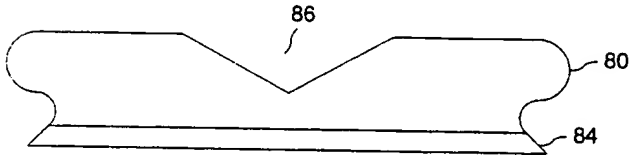


FIG. 4B

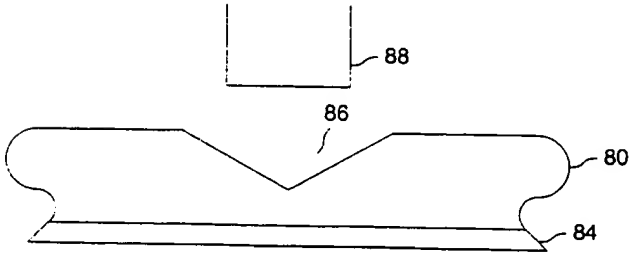


FIG. 4C

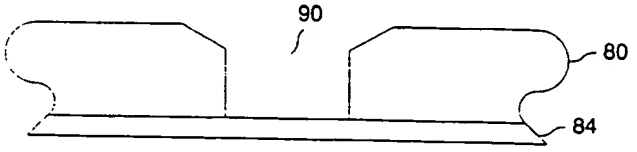


FIG. 4D

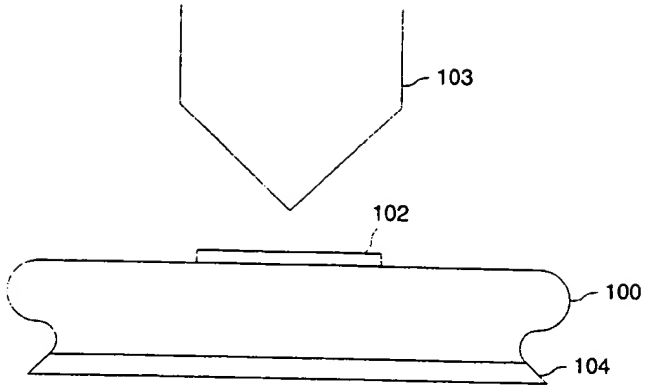


FIG. 5A

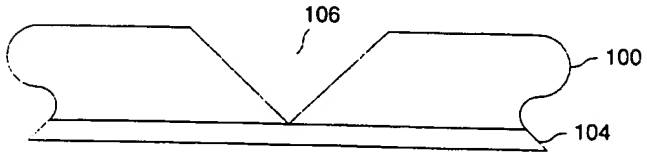


FIG. 5B

European Patent Office

# EUROPEAN SEARCH REPORT

Application Number
EP 95 30 2264

## DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document with indication, where appropriate, of relevant passages | Relevant to claim | CLASSIFICATION OF THE APPLICATION (Int.Cl.6) |
|---|---|---|---|
| X | PATENT ABSTRACTS OF JAPAN vol. 009 no. 321 (E-367) ,17 December 1985 & JP-A-60 154639 (HITACHI SEISAKUSHO KK;OTHERS: 01) 14 August 1985, | 1,3,5,6, 11,12,14 | H01L21/304 |
| Y | * abstract * | 2,4,7,9, 10,13 | |
| Y | EP-A-0 032 801 (TOKYO SHIBAURA ELECTRIC CO) 29 July 1981 * abstract; figure 7 * | 2,13 | |
| Y | US-A-4 851 371 (FISHER ALMON P ET AL) 25 July 1989 * column 6, line 51 - line 62; figures * * column 8, line 3 - line 41 * | 7,9,10 | |
| Y | US-A-5 000 811 (CAMPANELLI MICHAEL R) 19 March 1991 * column 3, line 33 - line 48; figure 1A 1B * | 4 | |
| A | EP-A-0 228 863 (SEIKO INSTR & ELECTRONICS) 15 July 1987 * abstract; figures 1A-1C * | 1,7,9,10 | TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L |
| A | IBM TECHNICAL DISCLOSURE BULLETIN, vol. 34, no. 12, 1 May 1992 pages 311-312, XP 000308530 'METHOD OF PREVENTING DAMAGE TO INTEGRATED CIRCUIT CHIPS DURING WAFER DICING' * the whole document * | 1,2 | |
| A | EP-A-0 438 127 (TOKYO SHIBAURA ELECTRIC CO ;TOSHIBA MICRO ELECTRONICS (JP)) 24 July 1991 * the whole document * | 1,2 | |

The present search report has been drawn up for all claims

| Place of search | Date of completion of the search | Examiner |
|---|---|---|
| BERLIN | 21 July 1995 | Roussel, A |

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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P : intermediate document

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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